

Amendments to the Specification:

Please replace paragraph [0001] with the following:

This application is related to co-pending U.S. Patent Application No. 10/713,878 (Attorney Docket No. 10829.8742US) filed on November 13, 2003, which is incorporated herein by reference in its entirety.

Please replace paragraph [0030] with the following:

The microelectronic dies 220 can further include a plurality of conductive links 228 extending between the first surface 226 and the second surface 227. The conductive links 228 shown in Figure 3 are through-wafer interconnects electrically coupled to corresponding bond-pads 224. The ends of the conductive links 228 proximate to the second surface 227 define a plurality of pads 229. The through-wafer interconnect type conductive links 228 can be formed by laser drilling holes through the dies 220, depositing a dielectric layer along the sidewalls of the holes, spacer etching the dielectric layer, and then filling the holes with a metal. Suitable processes for forming the interconnects are disclosed in co-pending U.S. Application No. 10/713,878, entitled Microelectronic Devices, Methods for Forming Vias in Microelectronic Devices, and Methods for Packaging Microelectronic Devices, filed on November 13, 2003 (Perkins Coie Docket No. 10829.8742US00). In other embodiments, the microelectronic dies 220 may not include conductive links 228, or, alternatively, the conductive links 228 may not extend through the bond-pads 224. In still other embodiments, the conductive links 228 can extend along the side of the dies 220 in the area between the dies.